1st International Workshop on **Hardware Acceleration of Functional and Declarative Languages**

Call for Participation

The call for participation in the 1st International Workshop on Hardware Acceleration of Functional and Declarative Languages (HAFDAL) is now open.

HAFDAL '24 is hosted in conjunction with the International Symposium on High-Performance Computer Architecture (HPCA) 2024 — see hpca-conf.org/2024/ for details. The event will be hosted in Edinburgh, UK, March 3rd 2024.

Submission

The 1960s and 1970s saw LISP machines for supporting AI workloads. The 1980s saw graph reductions machines for functional language workloads. After a 30 year lull, modern hardware technology has attracted renewed interest in hardware acceleration of high level languages. This workshop brings together computer architects and programming language implementers to identify software/hardware co-designs of these high level execution models.

This workshop invites two forms of participation: (1) full submissions for 30 minute talks, (2) 5-10 minute lightning talks about related projects and early results. Please send an abstract to craig.ramsay@hw.ac.uk by November 20th 2023. We are looking for submissions that cover the motivation, design, or real-world application of hardware technology for functional/declarative languages, their compilers and runtime systems. The work should target truly custom (e.g. ASIC/FPGA) hardware, or exploit modern hardware features for functional/declarative language implementation, across the design space of:

- Special-purpose processor architectures for functional or declarative languages.
- Automatic, high-level synthesis of custom accelerators from plain, high-level software functions.
- Hardware description languages embedded in, or hosted by, high-level software languages.

Key Dates

Submission deadline 20 November 2023

Author notification 18 December 2023

Final manuscript due 15 January 2023

Workshop 3 March 2024

Please email inquiries concerning the workshop to: craig.ramsay@hw.ac.uk.